REMARKS

Entry of this Amendment in accordance with the provisions of 37 C.F.R. §1.114 is respectfully requested.

This Amendment is in response to the Office Action dated December 9, 2003.

By the present Amendment, independent claim 11 has been amended to incorporate the subject matter of its dependent claim 12 (which has correspondingly been cancelled). Similarly, independent claim 17 has been amended to incorporate the subject matter of its dependent claim 20 (which has also been cancelled). Each of the independent claims 11 and 17 have also been amended to delete the limitations regarding the material of the insulating film and the gate electrode since these are not necessary to define over the cited prior art. These limitations have been added, instead, as new dependent claims 21-24. In addition, new independent claim 25 and dependent claims 26 and 27 have been added to define the invention from a different perspective, as will be discussed below.

Reconsideration and the removal of the objections to independent claims 11 and 17 is respectfully requested. By the present Amendment, each of these claims has been amended to overcome the minor objections raised under the heading "Claim Objections" in the Office Action. Therefore, removal of these objections is respectfully requested.

Briefly, the present Amendment emphasizes a feature of the invention previously defined in dependent claims 12 and 20. As discussed in the last Amendment filed on September 15, 2003, the present invention utilizes a plurality of microcrystal grains A8, shown, for example, in Fig. 1, covered with insulating films such as A7 and A10. By virtue of this, each of the microcrystal grains A8 operates

as an independent and electrically disconnected charge storage region. A major advantage of this aspect of the present invention is that, if cracks develop in the insulating films A7 and A10, leakage would be limited to an isolated microcrystal grain A8, while the other microcrystal grains A8 continue function properly as charge storage areas.

In addition, the inventors have discovered that by using this structure, in conjunction with the setting of thickness of the insulating layers, it is possible to transfer charge accumulating in the silicon microcrystal grains A8 not only between the substrate and the microcrystal grains, but also between the microcrystal grains and the gate electrode A9 (e.g. see page 10, lines 16-20). In each case, the transfer of charge is controlled by the potential provided at the gate electrode. Thus, Applicants have discovered that the electric potentials applied to the gate electrode A9 both for writing data and for erasing data can actually have the same polarity. This is a great advantage in terms of simplifying the power generating circuit for the gate electrode, and significantly reduces the area of the peripheral circuitry, as discussed on page 11, line 8 through page 12, line 7. Specifically, as shown in the Table on these pages, a +5 volts can be used for writing data and +10 volts can be used to erase data (see also page 8, line 2 through page 9, line 16).

Reconsideration and allowance of amended independent claims 11 and 17 over the cited combination of Flagan and Sadd is respectfully requested. Regarding this, although Flagan may initially appear to be similar to the present invention in terms of using isolated cores 102 between a channel region 120 and a gate electrode 132, a careful examination of the reference shows that it is, in fact, quite different in terms of the feature added to each of independent claims 11 and 17 that:

> "wherein an electric potential to be applied to said gate electrode upon writing of data and an electric potential to be applied to said gate electrode upon erasing of data have the same polarity."

More specifically, in the Office Action, it is noted that Flagan teaches on column 15, lines 19-23 that the same gate potential of +8 volts can be used for both writing and erasing data. After carefully reviewing this matter, the inventors respectfully submit that this is obviously a misprint or a typographical error in Flagan since it is in direct conflict with the rest of Flagan's disclosure regarding the writing and erasing operations, particularly Figs. 14 and 15, as will be discussed below.

For example, Fig. 14 of Flagan shows the data rating operation. As can be seen in Fig. 14, the substrate voltage is held at –5 volts, and each of the illustrated gate voltages is a positive voltage (ranging from a +4 volts to +10 volts). On the other hand, in Fig. 15, which is the erasing operation, the substrate voltage is +8 volts and all of the gate voltages are negative, specifically –10 volts to –4 volts. As such, the graphs of Figs. 14 and 15 of Flagan clearly show that a positive gate voltage is used for writing and a negative gate voltage is used for erasing. Thus, it is clear that the description found on column 15, lines 19-23 describing the +8 volt gate voltage for writing and erasing regarding Figs. 14 and 15 must be a typographical error or misprint since it goes directly against the illustration in the figures which it describes. It would appear that what was actually intended on column 15, lines 21-23 of Flagan is regarding the erasing shown in Figs. 15 was:

> "The device erases to a low Dt of about +1V in 100 ms with gate and substrate bias of –8V and +8V, respectively." (underlining added for emphasis).

This would accurately correspond to Fig. 15, which clearly shows a negative gate voltage and a positive substrate voltage for erasing, opposite to the voltages used in Fig. 14 for writing.

For reasons set forth above, it is respectfully submitted that amended indpendent claims 11 and 17, both defining the use of the same gate polarity for writing and erasing, is actually directly opposite the teachings of Flagan. The Sadd reference adds nothing to Flagan to suggest any modification of Flagan to arrive at the claimed invention. More specifically, Sadd gives no suggestion whatsoever utilizing the same polarity gate voltage for both writing and erasing. Accordingly, reconsideration and allowance of the independent claims 11 and 17, as well as their dependent claims, is respectfully requested.

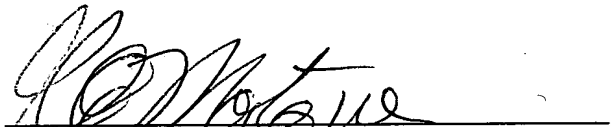
Reconsideration and sllowance of new independent claim 25 and its dependent claims 26 and 27 is also respectfully requested. These claims define the features of the present invention regarding both the independent charge storage and permitting data writing and erasing with the same polarity voltages in means plus function format. It is respectfully submitted that absolutely nothing in either Flagan or Sadd at all suggests these two functional features, particularly when considered in combination of the other elements of independent claim 25 and its dependent claims 26 and 27. Quite to the contrary, Flagan teaches thicknesses between the cores 102 and the gate electrodes which would be too thick to permit any transfer of charge stored between the cores and the gate electrodes that would be necessary to achieve writing and erasing of data using the same polarity voltages. Accordingly, reconsideration and allowance of new independent claim 25 and its dependent claims 26 and 27 is earnestly solicited.

If the Examiner believes that there are any points which can be clarified or otherwise be disposed of by way of a personal or telephone Interview, the Examiner is invited to contact applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage of fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, No. 01-2135 (Application No. 520.41287X00), and please credit any excess fees to said deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

By 
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